JOINT INVENTORS

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APPLICATION FOR UNITED STATES LETTERS PATENT

SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

Be it known that We, **Hoon Jang**, a citizen of Republic of Korea, residing at #A-1303 Deokseong APT., Bokdae 1-dong, Heungdeok-gu, Cheongju-si, Chungcheongbuk-do, 361-810, Korea; and **Keun Hyuk Lim**, a citizen of Republic of Korea, residing at #102 Na-dong, Mia 9-dong 133-1, Gangbuk-gu, Seoul 142-809, Korea have invented a new and useful **METHODS OF MAKING SHALLOW TRENCH-TYPE PIXELS FOR CMOS IMAGE SENSORS**, of which the following is a specification.

METHODS OF MAKING SHALLOW TRENCH-TYPE PIXELS FOR CMOS IMAGE SENSORS

TECHNICAL FIELD

[0001] The present disclosure relates to complimentary metal-oxide semiconductors (CMOS) and, more particularly, to methods of making shallow trench-type pixels for CMOS image sensors.

BACKGROUND

[0002] In a CMOS image sensor, a pixel detects an image by accepting light rays in an area on which a photodiode is formed. A photodiode is a device that produces electrical signals by generating electron hole pairs (hereinafter referred to as "EHPs") by means of incident light rays through a p-n junction.

[0003] At present, a commercialized process technology uses 0.35 micron (μm) ~0.50 μm technology, where a pixel size is 7~8 μm. In case of two-dimensional pixel architecture, in a process technology of 0.25 μm, the physical limit of pixel size is about 4 μm x 4 μm.

[0004] However, there is a technical problem in case of systems on chip (hereinafter referred to as "SoC"). In particular, SoC use a process technology of less than 0.25 μm to integrate many constituents on a single chip. Accordingly, the pixel size of a CMOS sensor must be reduced and the number of EHPs produced must remain at the existing level so that the sensor can separate image signals from noise and parasitic components.

[0005] A shallow trench isolation (hereinafter referred to as "STI") is one technique that can be used to isolate devices such as memory cells or pixels from one another. However,

STI methods may cause a dark current due to defect centers by etch damages around edges. To eliminate this disadvantage, the photodiode region is generally doped deeply by an ion-implanting process so as to cover the STI. However, in that case there is a problem in that signals with short wavelengths near blue region in visible rays get buried.

[0006] FIGS. 1a to 1c are cross sectional views illustrating a process of forming a pixel for a CMOS image sensor according to the prior art. Referring to FIG. 1a, a CMOS image sensor is formed on an epitaxial wafer having a structure of an epitaxial layer 2 doped with a low concentration positioned on a p-type substrate 1 doped with a high concentration. Active areas are isolated from one another by STI layers 3.

[0007] Next, referring to FIG. 1b, after patterning a photoresist layer 4 on the active area formed, an ion implantation process is conducted in order to form a photodiode p-n junction. There is a profile 6 doped in the epitaxial layer 2 doped with a low concentration.

[0008] Then, referring to FIG. 1c, the photoresist layer 4 is removed, and an annealing process is performed. A final profile 7 doped in the epitaxial layer 2 forms a junction under the STI layer 3 to reduce a recombination current generated at the STI edge.

[0009] As mentioned above, the existing method for making a pixel for a CMOS image sensor has to make a deep photodiode junction because of a recombination current problem due to defects and damages of STI edges. However, in that case, the signals of blue wavelength appear near the surface. In addition, in a two-dimensional structure the active area and pixel size are the same, and, therefore, a degree of integration is reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIGS. 1a through 1c illustrate, in cross-sectional views, the process steps according to a prior art pixel-fabricating method.

[0011] FIGS. 2a through 2d illustrate, in cross sectional views, the process steps according to the disclosed pixel-fabricating methods.

[0012] FIG. 3 is a layout of a pixel according to the disclosure.

[0013] FIG. 4 is a cross-sectional view of FIG. 3 taken along lines A-A'.

[0014] FIG. 5 is an equivalent circuit of a photodiode.

DETAILED DESCRIPTION

[0015] Referring to FIG. 2a, a CMOS image sensor is formed on an epitaxial wafer having a structure formed by an epitaxial layer 12 doped with a low concentration and positioned on a p-type or n-type substrate 11 doped with a high concentration. An active area is isolated from other active areas by a STI layer 13.

[0016] Referring to FIG. 2b, a photoresist layer 14 is coated over the structure of FIG. 2a. Then, a patterning process is conducted to form a shallow trench, and the epitaxial layer 12 is etched. The shallow trench may have a depth between about 10 angstroms (Å) and about 10,000 Å. The shallow trench may be filled with dielectrics such as oxide, nitride, oxinitride, and silicate glass by spin coating, chemical vapor deposition (CVD), or diffusion method.

[0017] Next, referring to FIG. 2c, a photoresist layer 15 is coated over the structure of FIG. 2b. Then, a patterning process is conducted to form a photodiode junction in the pixel

area formed, and an ion-implanting 16 is performed. Reference number 17 is a profile doped in the epitaxial layer 12 doped with a low concentration.

[0018] Referring to FIG. 2d, the photoresist layer 15 is removed and an annealing process is performed. A final profile 18 doped in the epitaxial layer 12 is formed through the annealing process. The annealing is performed by the rapid thermal annealing (hereinafter referred to as "RTA") or furnace annealing in the temperature range of 50~400 degree Centigrade (C).

[0019] FIG. 3 is a layout of a pixel according to the disclosed examples. A pixel 21 and a shallow trench 22 have been formed in an active area.

[0020] FIG. 4 is a cross-sectional view of FIG. 3 taken along lines A-A'. The reference number 23 is an epitaxial layer playing a role of a substrate, and reference number 24 is a doping profile of a photodiode.

[0021] FIG. 5 is an equivalent circuit of a photodiode. The disclosed methods can be applied to multi-transistor image sensor structures as well as a one-transistor image sensor structure.

[0022] Thus, the method for making of shallow trench type pixel for CMOS image sensor according to the disclosed examples can compensate reduction in the active area of a pixel using the area of the lateral wall of a shallow trench formed by etching the pixel area, although the design size of a pixel is reduced. Moreover, in an ion-implanting process to form a photodiode, the doping profile around the edge of the shallow trench is formed

deeply toward the lateral wall of the STI layer, thereby having an effect of a reduction of recombination current.

[0023] The foregoing disclosure is merely for example purposes and are not to be construed as limiting. The present teachings can be readily applied to other types of apparatuses. The disclosure is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those having ordinary skill in the art.

[0024] The foregoing disclosed methods for making a shallow trench type pixel for a CMOS image sensor substantially obviate one or more problems due to limitations and disadvantages of the related art. The disclosed methods include making a shallow trench type pixel, which can secure a minimum number of photoelectrons for processing video signals by increasing the active area of a pixel through forming a photodiode in the shape of a shallow trench in order to solve the problems due to a reduction in the number of photoelectrons according to a pixel shrinkage in a deep submicron level, i.e., a less than 0.25 μm technology for a CMOS image sensor.